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PACKET RADIO COMMUNICATIONS PROJECT

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13 ABSTRACT

Four major areas of activities in support of packet radio communications are reported on in this document. These are: (1) description of software and operating system in the first experimental repeater; (2) description of rf head in first experimental repeater; (3) description of overall mechanical design of first experimental repeater; and (4) discussion of equipment configuration to realize various experimental network elements in the experimental test bed.

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SUMMARY

A. TECHNICAL PROBLEM

This project is one part of a larger effort directed at extending packet switching technology into the area of radio communications. The technical investigations are focused on a Packet Radio Network (PRN) to serve fixed and mobile digital terminals in a tactical command and control environment. The objectives of the Collins investigations are:

- Perform research covering the application of radio frequency technology to packet switched communications.
- Participate in the overall ARPA Packet Communications Technology Program under the guidance of the Packet Radio Communications Working Group.
- Develop experimental equipments to support the Packet Radio System/Network experiments.
- Recommend a system architecture to provide terminal-to-terminal security for the packet-switched radio network.

B. GENERAL METHODOLOGY

The approach to the packet radio investigations is a combination of theoretical studies, equipment design efforts, and laboratory experiments. Work has been directed in each of the following areas:

- Experimental Equipment Design and Build. Detailed design and assembly of the experimental repeater described in the quarterly report, "Technical Plan for the Packet Radio Experimental Repeater," July 1974. This effort includes both hardware and software development.
- Communications Security. Evaluation of the impact of encryption and traffic flow security requirements and disciplines on system design. Development of a system architecture and design guidelines for an end-to-end encryption capability for Packet Radio Networks.

The above studies and design efforts are organized as an interactive process to achieve a proper balance between system performance and the constraints of available technology.

C. TECHNICAL RESULTS

This quarterly report treats four topics that have been investigated and developed during the reporting period in support of the experimental packet radio repeater development. The results of work done in communications security are reported under separate cover.

Specific technical results reported in this document include the following:

1. A functional description of the software being developed for the experimental packet radio repeaters.

2. A description of the rf head to be incorporated into the experimental repeaters. Test data on the transmitter and front-end receiver performance are included.

3. A description of the mechanical structure and assembly of the experimental repeater.

4. A discussion of experimental equipment configurations for network elements as they might be used for various applications in the experimental test bed.

D. PLAN FOR NEXT QUARTER ACTIVITIES

The emphasis during the next quarter will be to complete the integration, test, documentation, and delivery of the first three experimental repeaters for the packet radio test bed. Investigations of communications security for the packet radio network will continue. In addition, detailed investigations of specific issues affecting the radio system design (ie, mobile link characteristics, coexistence strategies, channel organization and management) will be addressed.

Section 1

Introduction

The first experimental packet radio repeaters are in the final stages of development and integration. At this point, test data have been gathered on various modules and subassemblies, the software structure is being finalized, and the mechanical configuration of the repeater has been decided. This report provides a compilation of some of this test data, a functional description of the repeater software, and a brief mechanical description of the repeater. It also contains an inventory of the hardware and software elements that make up the experimental repeater, along with discussions of the functional capabilities of each of these elements. Possible configurations of these elements to perform various functions in the experimental network are described.

Section 2 provides a description of the software organization for the experimental repeater. A description of the rf head, comprising significant portions of both the radio transmit and receive chains, is presented in section 3 complete with test data. Section 4 presents a brief mechanical description of the repeater. Finally, section 5 discusses the hardware and software elements in the experimental repeater and addresses the issue of what elements are needed to perform particular functions in the experimental network.

2.1 PURPOSE AND SCOPE

This section provides a functional description of the software being developed for the experimental packet radio repeater. This software will serve as a developmental operating system to be used for system testing, to support testing at Stanford Research Institute, and as the operating system used by the packet protocol and processing software elements to be developed by Network Analysis Corporation in cooperation with Collins Radio Group. Additionally, the operating system design permits utilization of the experimental repeater as a front-end to a station and/or terminal in the packet radio network experiments.

This section is preliminary in that it describes development work in progress. It will be modified and expanded to become an experimental repeater user's guide to be delivered with the experimental repeaters.

2.2 ORGANIZATION AND OPERATIONAL DESCRIPTION

The major elements of the software system for the experimental repeater are illustrated in figure 2-1. All elements shown are being developed by Collins with the exception of the packet control preprocess program and packet header process routines, which are being developed wholly or in part by Network Analysis Corporation. These programs, in general, define the packet protocols and high level packet input/output (I/O) control to be incorporated into the experimental repeater. Collins is providing the experimental repeater operating system, system test and debug aids, and software interfaces to the repeater hardware.

2.3 PROCESSING IN THE EXPERIMENTAL REPEATER

The software system is a multiprogrammed, interrupt-driven system; multiprogrammed in the sense that two independent programs may coexist in the system, and the state of the system is saved as control is transferred from one program to another. The system is interrupt-driven in that program control is transferred and processing initiated as a result of CPU interrupts.

The system is structured into three processing modes defined as foreground, background, and executive. Figure 2-2 illustrates the assignment of processing tasks within the processing modes and transfer of control between modes.

The executive mode is utilized for system initialization, mode control, and system test and debug aids. In general, the executive mode is noninterruptable for foreground and background processing. Transfer of control between the foreground and background modes is through the executive mode, which saves and restores the state of the foreground/background modes as represented by the CPU; program counter, registers, status, and stack. The executive determines when to remove power to selected repeater hardware elements and reinitiates processing when power is restored. Programs which operate in the executive mode include the following.

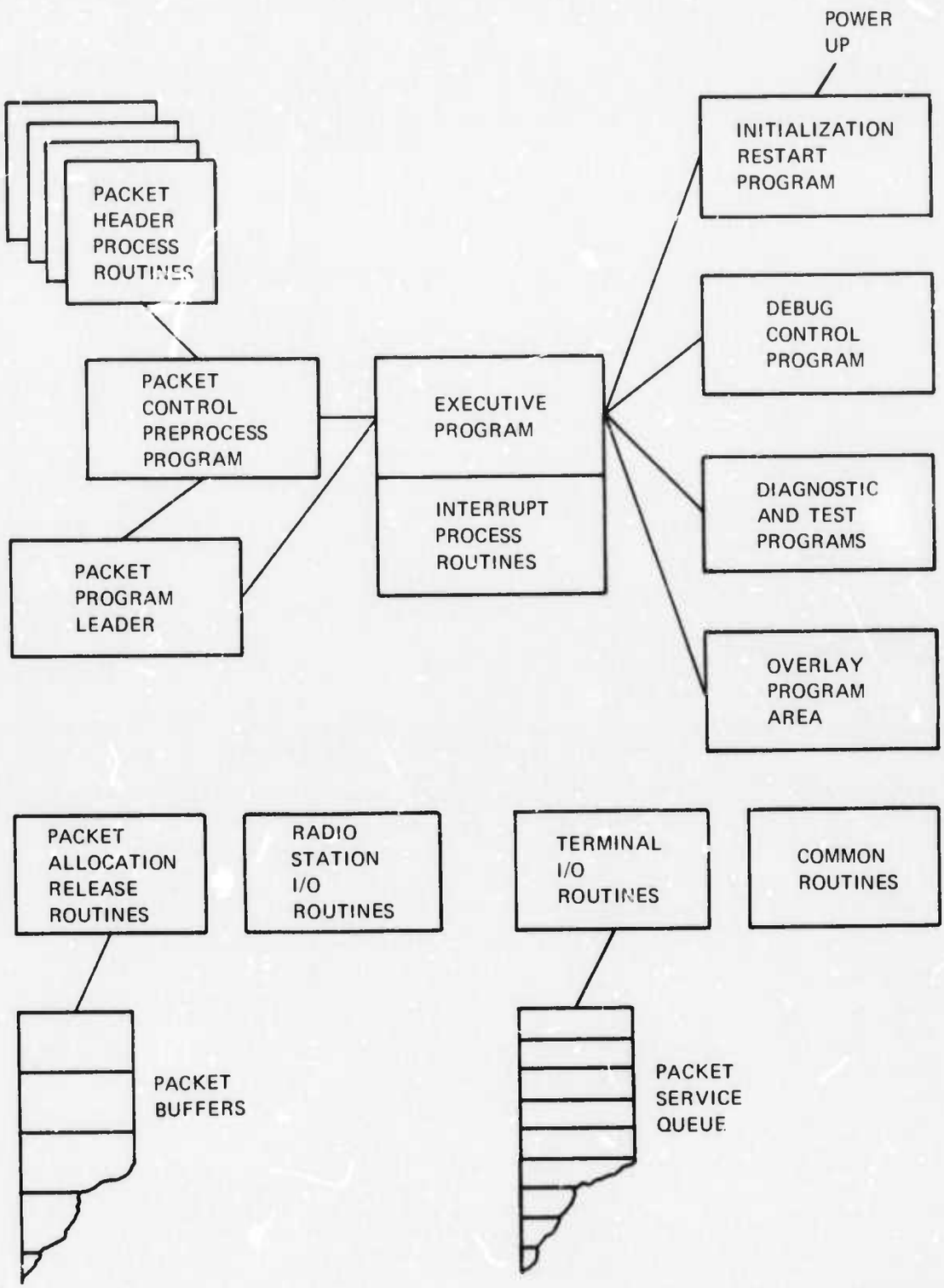

Figure 2-1. Experimental Repeater Software.

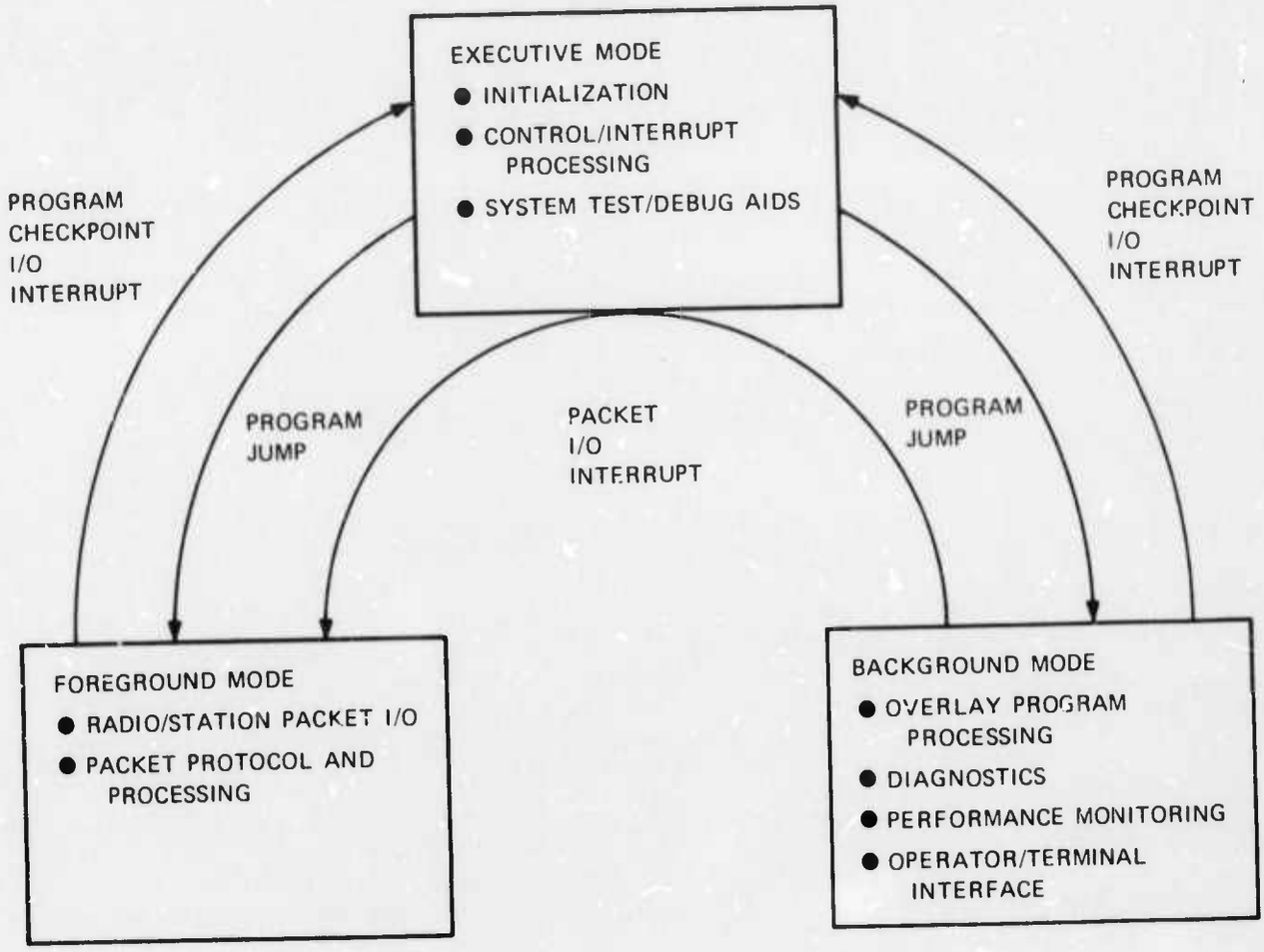

Figure 2-2. Experimental Repeater Processing Organization.

a. Executive program

b. Interrupt process routine

c. Initialization/restart program

d. Debug/control program.

The foreground processing mode is utilized for radio and station packet I/O and processing. The foreground mode programs retain control until packet I/O and processing is temporarily completed, and then programs release control by checkpointing to the executive. They regain

control upon the occurrence of a DMA channel interrupt indicating the completion of a packet I/O and, thus, the need for packet processing. The foreground mode is interrupted periodically to service character I/O to the terminal. The foreground programs in the experimental repeater include the following:

a. Packet control preprocess program

b. Packet header process routines

c. Packet program loader

d. Radio/station I/O routines.

The background processing mode is utilized for overlay programs, on-line diagnostics, performance monitoring, and later operator/terminal interaction programs in the packet radio network terminal. Overlay programs include programs that are contained in packets and are executed and then overlayed. This feature will serve to reduce memory requirements for resident software in the repeater.

The remaining software elements illustrated in figure 2-1 may be utilized by all process modes and assume the current process mode when called for execution. These programs include:

a. Packet allocation/release routines

b. Terminal I/O routines

c. Common routines.

All interfaces between process modes and calls to commonly used routines are via indirect calls to memory base page. This simplifies program interfaces and provides a form of program relocation capability via modification of base page contents.

2.4 MEMORY MANAGEMENT IN THE EXPERIMENTAL REPEATER

The initial experimental repeaters will contain 1024 words of PROM and 3072 words of RAM memory. The PROM is utilized for the basic operating system which includes:

a. Initialization/restart program

b. Debug control program

c. Executive program

d. Interrupt routines (except for DMA channel)

e. Terminal I/O routines.

The base page (RAM locations 0 - 255_{10}) is utilized for program linkages, tables, jump tables, constants, and operational parameters. Approximately one-half of these locations are utilized by the Collins-developed operating system and programs. The remaining words are reserved for use by other programs.

Approximately 1500 words of RAM memory are utilized for the remaining elements of the operating system which include:

a. Base page

b. Four packet buffers

c. Radio/station I/O and interrupt routines

d. Packet allocation/release routines.

Thus, about 1500 words remain for use by the packet control preprocess program, packet header process routines, packet program loader, and overlay program area plus one-half of base page.

The off-line diagnostic and test support programs utilize the RAM memory area, but are overlayed when not in use.

2.5 OPERATIONAL PROCEDURES IN THE EXPERIMENTAL REPEATER

2.5.1 Initialization

The PROM memory software, when the repeater power is turned on, initializes base page and prompts the operator at the terminal. The full capabilities of the debug control program are at the disposal of the operator via appropriate terminal keyboard input and terminal display. Normally, additional programs will be loaded into RAM, utilizing the loaders resident in PROM. These programs may be off-line diagnostics, or the remaining elements of the operating system and the high level packet protocol and processing programs. The operator may then initiate, supervise, and control the operation of foreground and background programs via the repeater terminal.

2.5.2 Packet I/O and Processing

High level packet I/O control and protocol processing is accomplished by the packet control preprocess program and packet header process routines. In general, the packet control preprocess program will begin by requesting packet buffers via the packet allocation routine, and will request the enabling of radio (and station if implemented) receivers. The program may then release control (checkpoint) until receipt of a packet signified by a DMA channel CPU interrupt. The interrupt returns control to the foreground process mode where the packet control preprocess program calls the radio/station I/O routines, requesting the address of completed packets. Packet processing determines if the packet was received correctly, if it is addressed to the repeater, and decodes the packet type. The packet type is utilized to call the appropriate packet header process routine, where detailed processing of the packet header is completed and final disposition of the packet determined. The packet may be discarded by an echo acknowledge to prior packet, or may be transmitted to the radio or station by appropriate calls to packet I/O routines. In addition, the called receiver is reenabled to receive other packets.

In this manner packets are input/output and processed normally on a first-in/first-out basis.

The radio/station I/O routines are designed to permit the high level protocol software to request one packet I/O per implemented DMA channel packet I/O interface. They determine when to enable the appropriate transmitters and receivers based on other I/O activity and packet I/O parameters stored in memory base page. They detect completed packet I/O trans-

actions and supply upon request the associated packet buffer addresses to the high level software.

In summary, the packet control preprocess program and packet header process routines are responsible for requesting packet I/O, processing of the packet headers and final disposition of the packets, use of the packet buffer resource, and specification of the packet I/O parameters. The packet I/O, interrupt, allocation, and release routines are responsible for the real-time implementation of the packet I/O and appropriate use of the packet I/O parameters.

2.6 SOFTWARE OPERATING SYSTEM ELEMENT DESCRIPTION

The major software elements being developed by Collins, to be supplied with the developmental repeaters, are illustrated in figure 2-3. These elements provide a basic operating system to be utilized to support the radio packet algorithms, station and terminal interfaces, repeater hardware diagonostic programs, and software/hardware test and development.

Some of these software elements will be PROM resident, others will be loaded from the terminal (paper tape and/or tape cassette) as needed.

2.7 INITIALIZATION/RESTART PROGRAM

This program is responsible for initialization of the repeater software from a repeater power-off state. Two power-off states are possible: (1) power is totally removed from the repeater; (2) only selected high power consuming elements have power off. In the first case, the software initializes RAM basic page (first 256 memory locations) as required by the PROM resident software. Control is then passed to the debug/control program which prompts for operator input to the terminal.

In the second case, the software restores the CPU registers, status, and stack and restarts the programs being executed when power was removed. This power-off state is accomplished under software control. Power is restored as a result of a CPU interrupt from the DMA channels or terminal. This program is resident in PROM.

2.8 EXECUTIVE PROGRAM

The executive program implements the foreground and background processing modes and provides the path by which control is transferred from one mode to another. It saves and restores the machine state for the foreground and background processing modes as represented by the four CPU registers, status, stack, and program address counter.

The foreground and background programs pass control to the executive program when they have no current processing requirements, or control is passed automatically as a result of repeater input/output events.

Additionally, the executive program determines when to initiate partial repeater power shutdown and save the machine state for later restoration. This program is resident in PROM.

2.9 INTERRUPT PROCESS ROUTINES

The interrupt process routines are entered upon the occurrence of a CPU interrupt through memory location 0001. The interrupt register is read and interrupt souces decoded. Control is passed, in turn, to routines which service each interrupt detected. The interrupt sources are as follows.

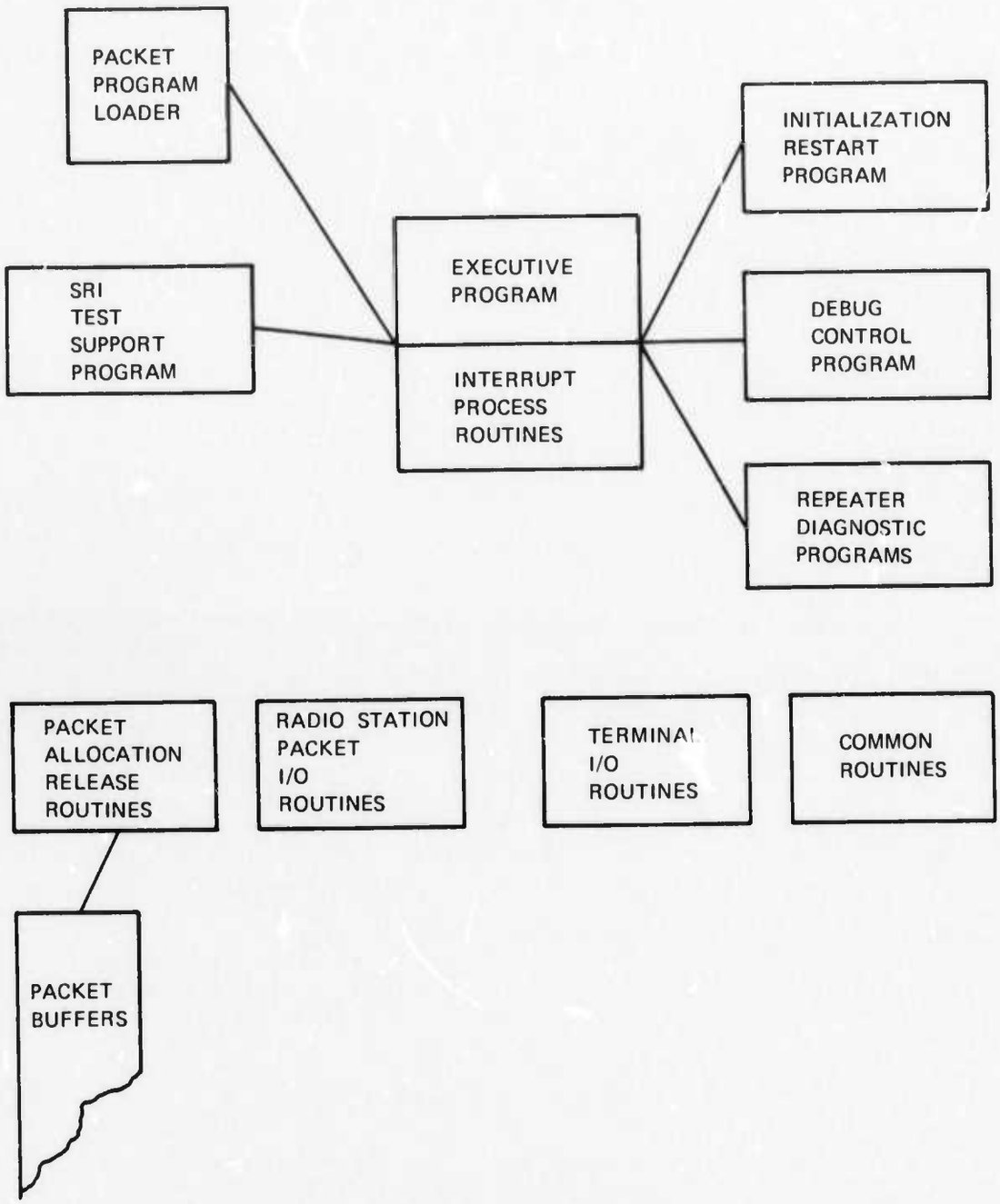

Figure 2-3. Developmental Repeater Software.

a. Time interval clock

b. Stack overflow

c. Manual (operator)

d. DMA channels (for radio, station I/O)

e. Terminal I/O channel.

All the interrupt process routines are resident in PROM except for the DMA channel routines in theinitial experimental repeaters.

2.9.1 Time Interval Clock Interrupt Routine

This routine adds one to a memory location in base page upon each clock interrupt. This memory word may then be utilized by programs to determine elapsed time. The memory location is incremented by 1 to a maximum value of $7FFF_{16}$ and reset to 0000_{16}. The clock interrupt interval is currently 131 ms.

2.9.2 Stack Overflow Interrupt Routine

This routine halts further forground or background processing and returns control via the executive program to the debug/control program where the operator may determine the causes of the stack overflow. Normally, this will result from a software error, but may be the result of a hardware failure.

2.9.3 Manual Interrupt Routine

This routine is identical to the stack overflow interrupt routine. It permits the operator to regain control of the repeater via activation of a pushbutton switch.

2.9.4 DMA Channel Interrupt Routines

There is one interrupt routine per implemented DMA channel: one for station input, station output, radio transmitter; and one each for the two radio receivers in the experimental repeater. DMA channel interrupts occur as a result of the beginning of data transfer for radio packet reception or upon completion of packet data transmit or reception on the radio and station DMA channels.

The interrupt routines place the address of the packet buffer associated with the interrupting DMA channel in the packet service queue and update the information in the packet buffer for use by the packet control preprocess program and packet header process routines. Additionally, these routines will initiate any pending DMA channel I/O now possible as a result of the completed DMA I/O operation. For example, if the packet transmision has been completed, any pending radio receiver DMA I/O is initiated. Finally, the DMA interrupt routines return control to the foreground processing mode so that processing may be initiated for the completed packet I/O operations.

2.9.5 Terminal I/O Channel Interrupt Routine

This routine inputs or outputs a single character to the terminal per interrupt. The I/O may be either binary or ASCII data. Additionally, the routine decodes message edit characters and recognizes the single character ENQ as an operator request to transfer control to the debug/control program.

2.10 DEBUG/CONTROL PROGRAM

The debug/control program provides the operator at the terminal with system supervisory control, and test and debug aids via appropriate terminal input and display. The program is executed upon completion of repeater initialization or upon occurrence of certain events during normal operation: for example, operator input of ENQ character and manual or stack overflow interrupt.

The program prompts the operator at the terminal, and the operator responds with desired control selections. The following are the operator directed functions.

a. Initiate foreground and/or background programs at defined locations.

b. Display and modify foreground/background; program counter, registers, status and stack.

c. Select program breakpoints for software trace debugging.

d. Display and modify selected memory locations and peripheral I/O interface registers.

e. Load bootstrap or absolute (nonrelocatable) RLM format programs from the terminal. These formats are as defined by National Semiconductor Corporation for the IMP-16P.

f. Dump (create) bootstrap format programs to the terminal.

g. Halt (idle and clear) forground/background programs.

This program is resident in PROM.

2.11 PACKET ALLOCATION AND RELEASE ROUTINES

These routines provide a packet buffer or return a packet buffer to the packet buffer pool upon request of the packet preprocess and control program or other programs requiring packet buffer space.

The routines are accessible via indirect subroutine call through the memory base page. The system currently provides four packet buffers in the experimental repeater. These routines are currently resident in RAM.

2.12 RADIO/STATION PACKET I/O ROUTINES

These routines implement packet I/O as requested by the packet protocol, process, and various test programs, and provide upon request the packet addresses of completed packet I/O.

2.12.1 Use of Packet I/O Routines

Packet I/O and other processes are requested via indirect subroutine call through the memory base page. The user provides the packet buffer address and modifies the packet buffer dispsoition word to define the desired packet I/O. The I/O routines, in turn, insert information into the packet buffer to be used by the user programs to determine the status of the packet and initiate the requested packet I/O. The I/O routines will accept one packet I/O request per implemented DMA radio/station interface, and initiate the request immediately or queue the request for later initiation if current DMA activity prohibits immediate execution. For example, radio (ALOHA mode) transmit will not be initiated if radio receiver is inputting data,

but will be initiated when the data transfer is completed. If the radio receivers are enabled and not transferring data, they will be disabled and reenabled upon completion of transmit. Similarly, radio reception is not initiated if the transmitter is enabled. If the carrier sense transmit mode is selected, the I/O routines will enable idle radio receivers with dummy packet buffers to verify absense of carrier sense before transmitting.

Upon completion of packet I/O signified by DMA channel CPU interrupt, the associated packet buffer address is stored in the packet service queue. The user has access to these addresses via indirect subroutine call through memory base page.

2.12.2 Packet Buffer Format

The packet buffer format is illustrated in figure 2-4 and described in the following paragraphs.

a. Packet Chain Address. Address is of the next packet buffer in packet buffer queue. Packet buffer addresses in all cases point at first word of packet header/test.

b. Packet Identification. This is a unique code utilized by I/O routines to check validity of packet address.

c. Significant Event Check. Value is of the time clock (updated by clock interrupt routine) when packet status changes.

d. DMA Status/Control Register. Image is of the DMA channel status/control register when packet status is updated, and is used by I/O routines.

e. DMA Address Register. Image is of the DMA channel address register when packet status is updated.

f. Packet Status. Packet status, inserted by the I/O routines, is utilized by the high level software to determine the current state of the packet. The status indications are:

1. Idle - Unassigned
2. Idle - Assigned to User
3. TX/RX Pending (queued TX/RX)
4. TX/RX Initiated (assigned to enabled DMA channel)
5. RX in Progress (data transfer in progress)
6. TX/RX Complete
7. TX/RX Complete with Error.

g. Spare. Three words are reserved for future definition, two of which may be defined and used by the high level programs.

h. Packet Disposition. The packet disposition word is modified by the high level software to define the desired packet I/O to be executed by the I/O routines. The defined packet dispositions are as follows.

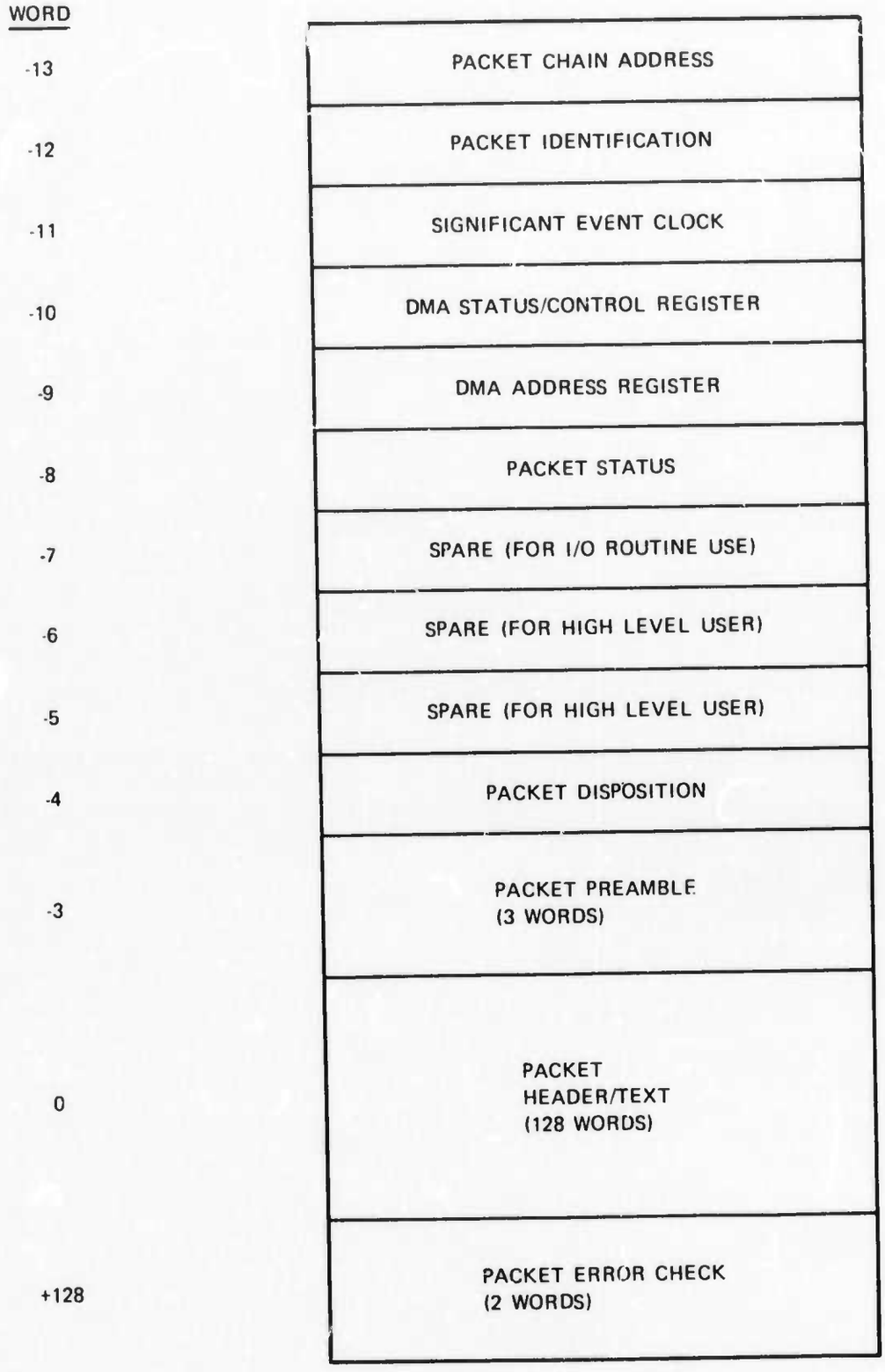

Figure 2-4. Packet Buffer Format.

1. Idle Packet (disable DMA and/or remove from queue)
2. Radio Transmit 100 KBIT Rate
3. Radio Transmit 400 KBIT Rate
4. Radio Receive 100 KBIT Rate
5. Radio Receive 400 KBIT Rate
6. Transmit to Station
7. Receive from Station.

i. Packet Preamble. Three words are transmitted to the radio to define the packet preamble code.

j. Packet Header/Text. Content is of the packet received and/or transmitted. A maximum of 128 words is provided for each packet.

k. Packet Error Check. Two words are received at end of the packet utilized by the repeater hardware to verity packet data.

2.12.3 Radio Transmit Parameters

Four words are defined in base page to specify radio transmit parameters. These may be modified by the packet protocol and process programs to control radio transmissions. These parameters are:

a. Radio Transmit Enabled/Disabled

b. Radio Transmit Mode - ALOHA, Carrier Sense, or Test

c. Radio Transmit Power Level

d. Radio Transmit Frequency.

2.13 TERMINAL I/O ROUTINES

The terminal I/O routines implement the transfer of data between the terminal and requesting programs. Initially, the routines will supprot a TTY keyboard, printer, and paper tape reader and punch terminal. Additional routines will be developed to utilize the Texas Instruments Silent 700 keyboard, printer, tape cassette terminal.

PROM memories will be programmed to support the terminal being used. The routines are accessible via indirect subroutine call through base page and return control to the user upon completion of the requested terminal operation. These routines/call provide the capability to:

a. ASCII message I/O to/from keyboard and printer

b. Binary data record I/O to/from the tape media

c. Scan for unsolicited keyboard input

d. Hold terminal for several calls (to resolve terminal contention)

e. Release terminal (inverse of above)

f. Print binary word as four hexadecimal characters preceded by two spaces.

2.14 COMMON ROUTINES

Resident in PROM are several routines and binary constants that may be used as required by the repeater programs. The routines are called by indirect subroutine call through base page. The constants are resident in base page. These routines provide the following:

a. Set Status Flag

b. Clear Status Flag

c. Complement Status Flag

d. Skip if Status Flag True

e. Encode Binary to ASCII (0-9, A-F)

f. Decode ASCII (0-9, A-F) to Binary

Constants resident in base page are:

$FF00_{16}$, $00FF_{16}$ and 0001_{16}, 0002_{16}, 0004_{16} .... 8000_{16}.

2.15 DIAGNOSTIC TEST PROGRAMS

Several diagnostic test and test support programs will be provided for initial repeater development and for repeater operational verification. These programs are not resident in the repeater memory, but are loaded via the terminal and executed as required. Operational control of the programs is exercised by the operator at the terminal keyboard, and all error reporting is made to the terminal printer.

The programs to be provided are:

a. CPU diagnostic test program

b. RAM diagnostic test program

c. Packet I/O diagnostic test program

d. SRI test support program.

The CPU diagnostic test program is the National Semiconductor Corporation IMP-16P test program modified to utilize the terminal.

The RAM diagnostic test program provides a comprehensive test of random access memory.

The packet I/O diagnostic test program provides a comprehensive test of the operation of the DMA channels, interfaces, and radio.

Testing is accomplished via concurrent transmit and receive of data through two DMA channels where the channels are connected back-to-back through various loopback paths provided by the DMA channels, interfaces, internal to the radio, and reception of the repeater's own transmissions. In addition, the option is provided for transfer of packets between two repeaters.

The SRI test support program will receive packets for radio transmisstion from the station and transmit to the station packets input on the radio receivers. The goal is to provide a transparent packet transfer media to support the SRI testing.

It is important to note that the packet I/O diagnostic program and SRI test support program utilize the normal software elements of the operating system.

Additional diagnostic information is provided by the operating system. In general, when failure is detected, control is transferred to the debug control program where, with use of program listings, the functional failure may be diagnosed.

The rf head is a solid-state, fully integrated unit contained within a single housing. Microwave integrated circuit (MIC) techniques have been used throughout to achieve significant size and weight advantages. A photograph of the completed unit is shown in figure 3-1 and a functional block diagram is presented in figure 3-2.

The module features a transmitter and a low noise receiver coupled to the antenna port through a microstrip circulator. The transmit chain consists of an up-converter and three sections of rf gain. Other functions include filtering to reduce mixer spurious products and two step-attenuators to provide up to 20-dB reduction of output power in 5-dB steps.

The receive section is protected at its input by a T/R switch-limiter that provides a minimum of 30-dB isolation when the module is in the transmit mode. During receive, the switch is turned off and signal flow is into the low-noise amplifier; however, it still provides a passive-limiting function so that the power level appearing at the amplifier's input will not exceed +13 dBm, which is well below the "damage" level. A down-converter, low-pass filter and if amplifier complete the receiver circuit.

Measured data showing the performance of the transmit chain is presented in figure 3-3. A minimum of 8 W was obtained across the entire operating band, with 9.5 W at midband. The spurious response for worst case was 43 dB down at 1765 MHz. The entire chain, at full power, draws 1.7 A maximum off of a 24-V line.

The receiver response is summarized in figure 3-4. The rf-to-if gain is approximately 31 dB with a 4.5-dB noise figure (rising to 5.0 dB at 1850 MHz). The 1-dB gain compression point measured at the if output port is approximately +2 dBm. The receive requires +15 V and 23 mA.

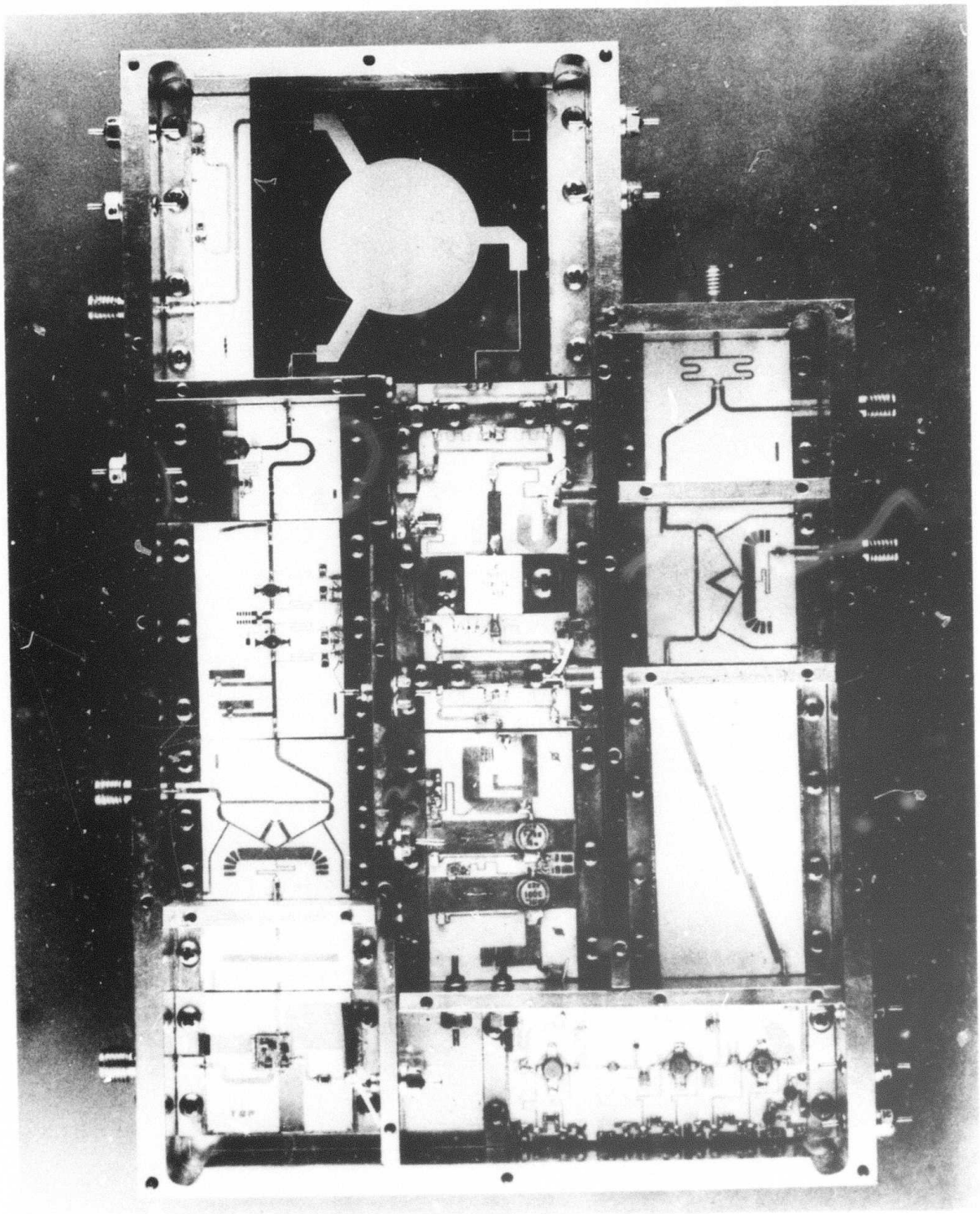

Figure 3-1. RF Head.

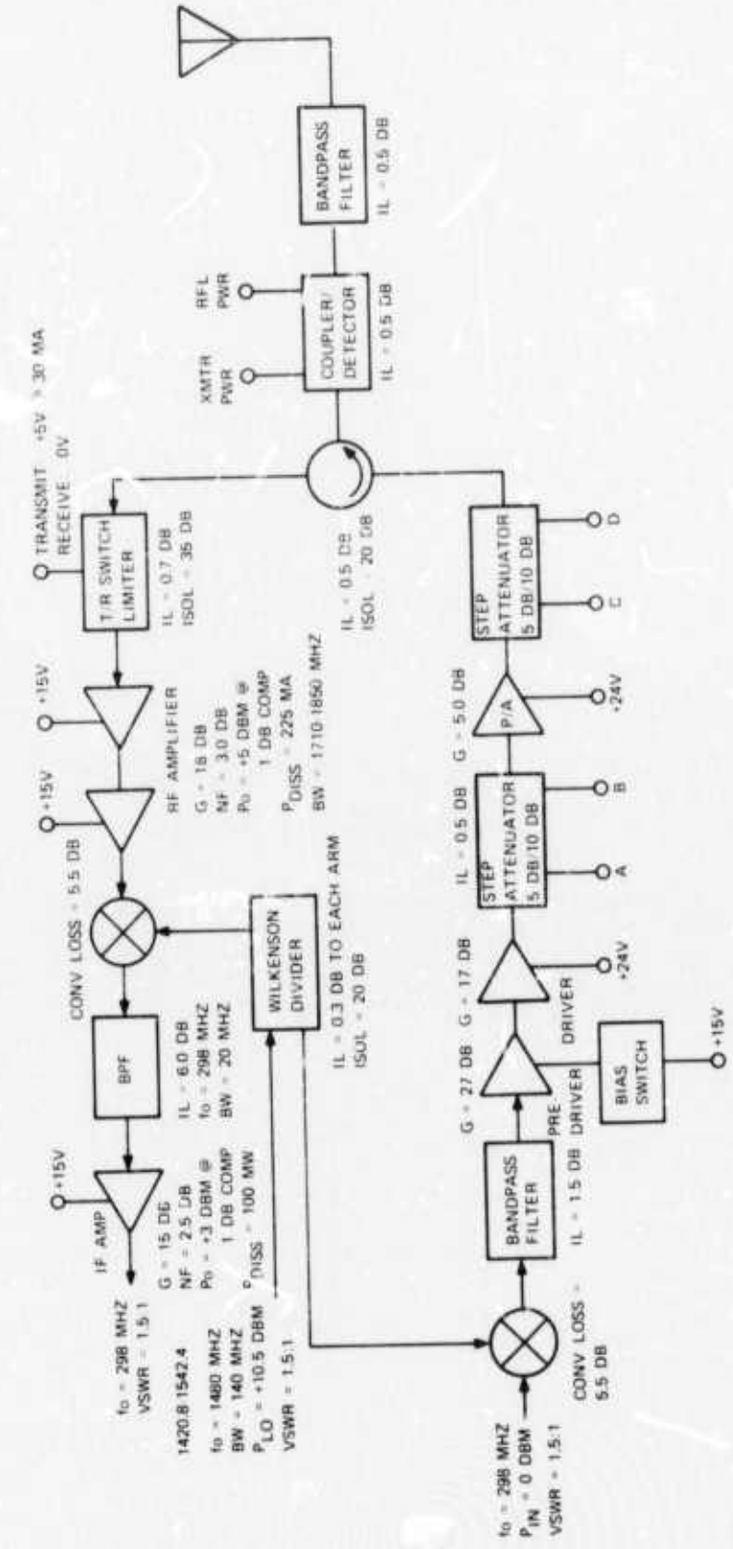

Figure 3-2. RF Subsystem, Functional Block Diagram.

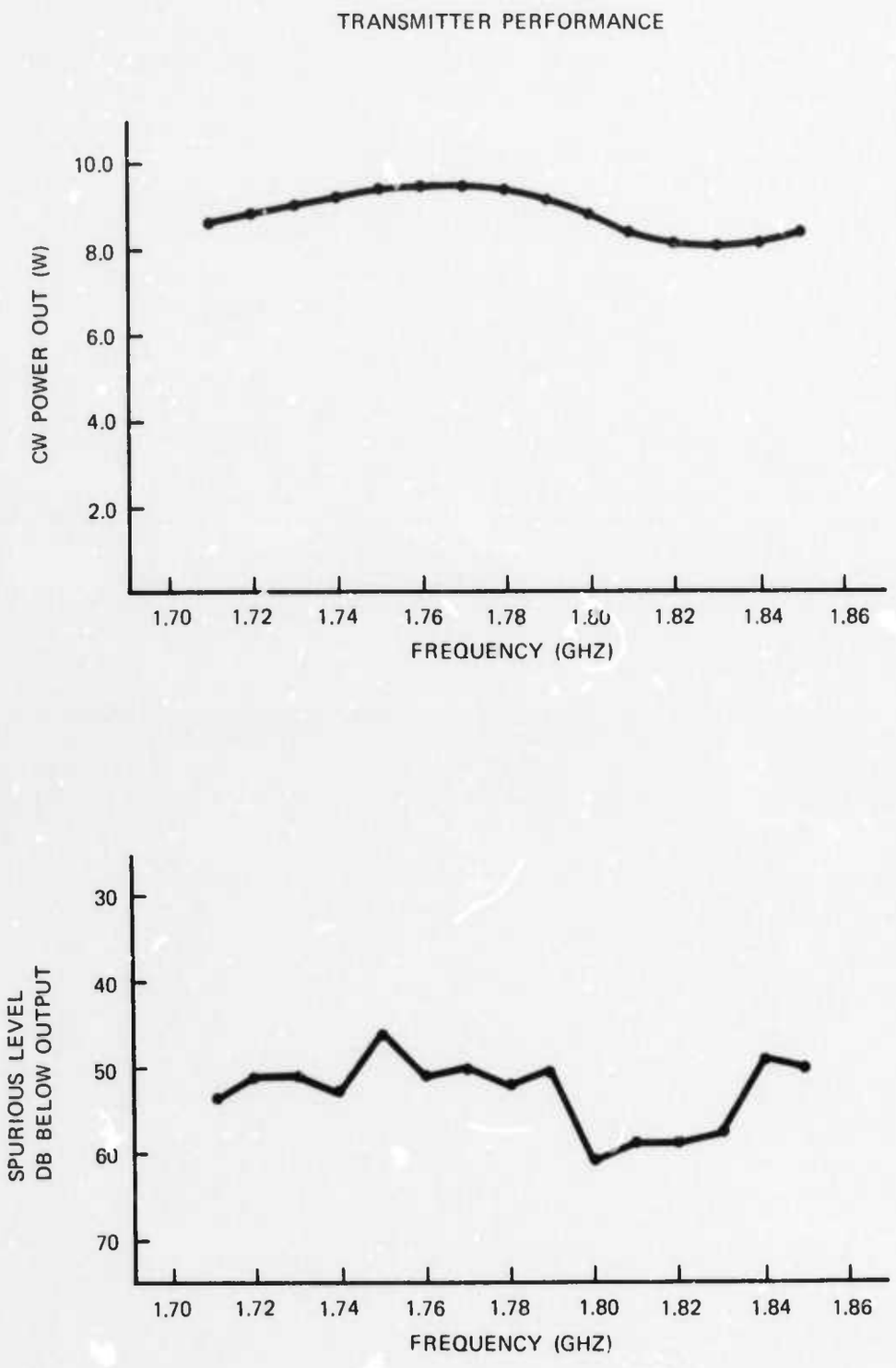

Figure 3-3. Transmit Chain Performance.

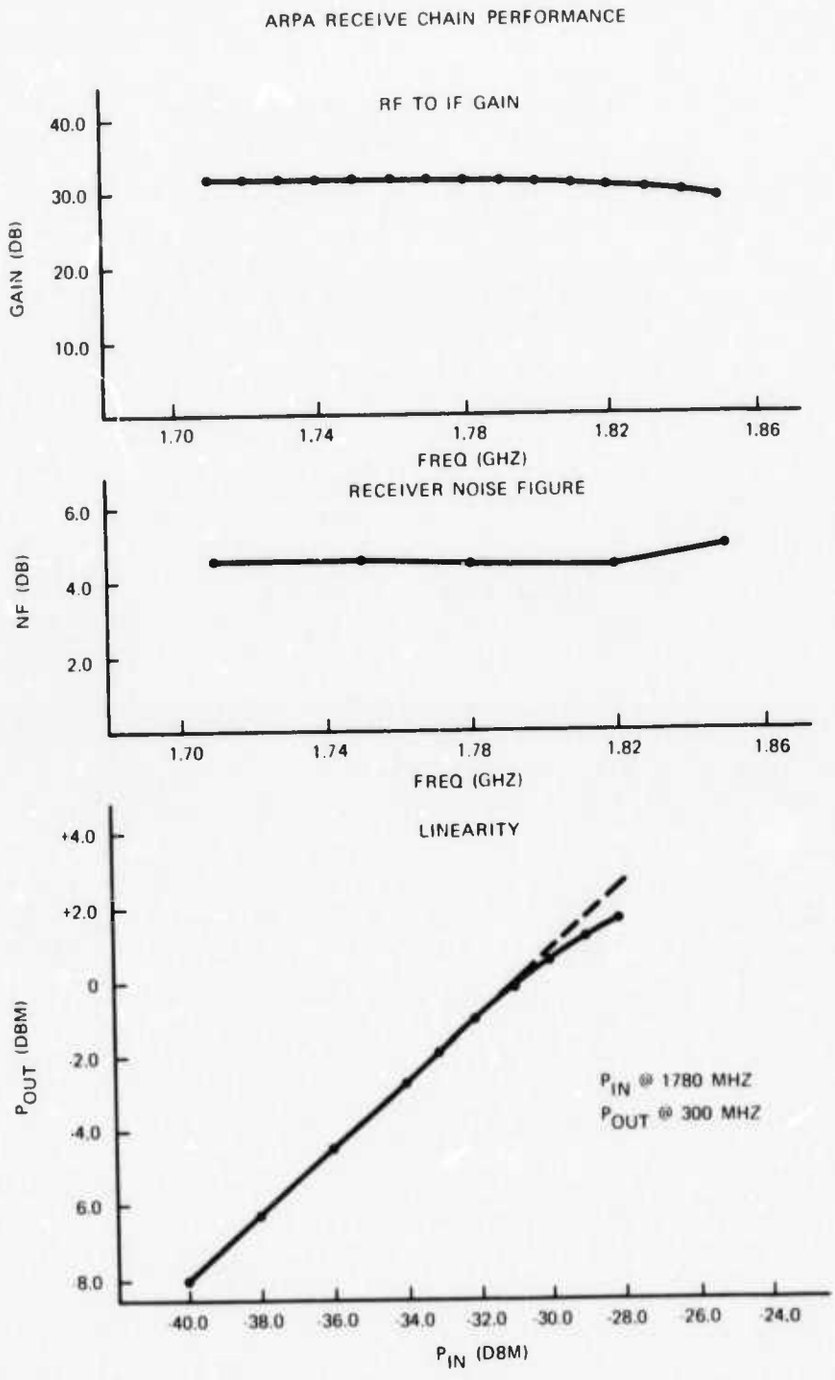

Figure 3-4. Receiver Response.

Mechanical Description of Experimental Repeater

The following is a brief description of the mechanical features of the experimental repeater. Figures 4-1 and 4-2 are views of the unit from the right front and left rear, respectively. The repeater has three major mechanical subassemblies: the chassis, the white finished box shown in figures 4-1 and 4-2; the rear cover assembly, the chromate finished finned section shown in figure 4-2; and the antenna, the tall cylinder atop the unit.

The entire unit, less antenna, measures 41.91 cm (16.5 inches) high, 27.94 cm (11.0 inches) deep and 29.46 cm (11.6 inches) wide.

The chassis is a raintight, white epoxy painted, sheet aluminum enclosure with a hinged and latchable front cover. The enclosure allows convection cooling through a perforated, screen covered bottom plate and a similar top plate. Rain is prevented from entering the top opening by an elevated, baffled top cover, as shown in figure 4-1. The front cover provides access to the front of the radio and digital card cages, and opening the cover allows removal of the modules for testing and service. The card cages are constructed of stamped and formed aluminum card guides. The radio card cage has an aluminum backplate mounting slide on coaxial connectors which mate with connectors on the radio modules. Behind the metal connector plane is a printed circuit backplane that mounts and interconnects the module printed board connectors. The digital card cage has only the printed circuit backplane for edge-on printed board connector mounting and interconnect.

The rear cover assembly, like the front cover, is hinged and latchable. The rear cover provides access to the rear of the radio and digital card cage printed circuit backplanes for maintenance and service. The rear cover is a finned plate with a metal shroud or wrap-around, and both are made of aluminum alloy.

The finned plate provides heatsinking for the rf module and repeater dc-to-dc converter which are mounted directly to the inside of the plate. Also mounted on the inside of the rear cover are the rf module filters and power supply filters, as well as the power connector and fuses on the input power lines as illustrated in figure 4-3. The antenna is mounted to the top of the rear cover.

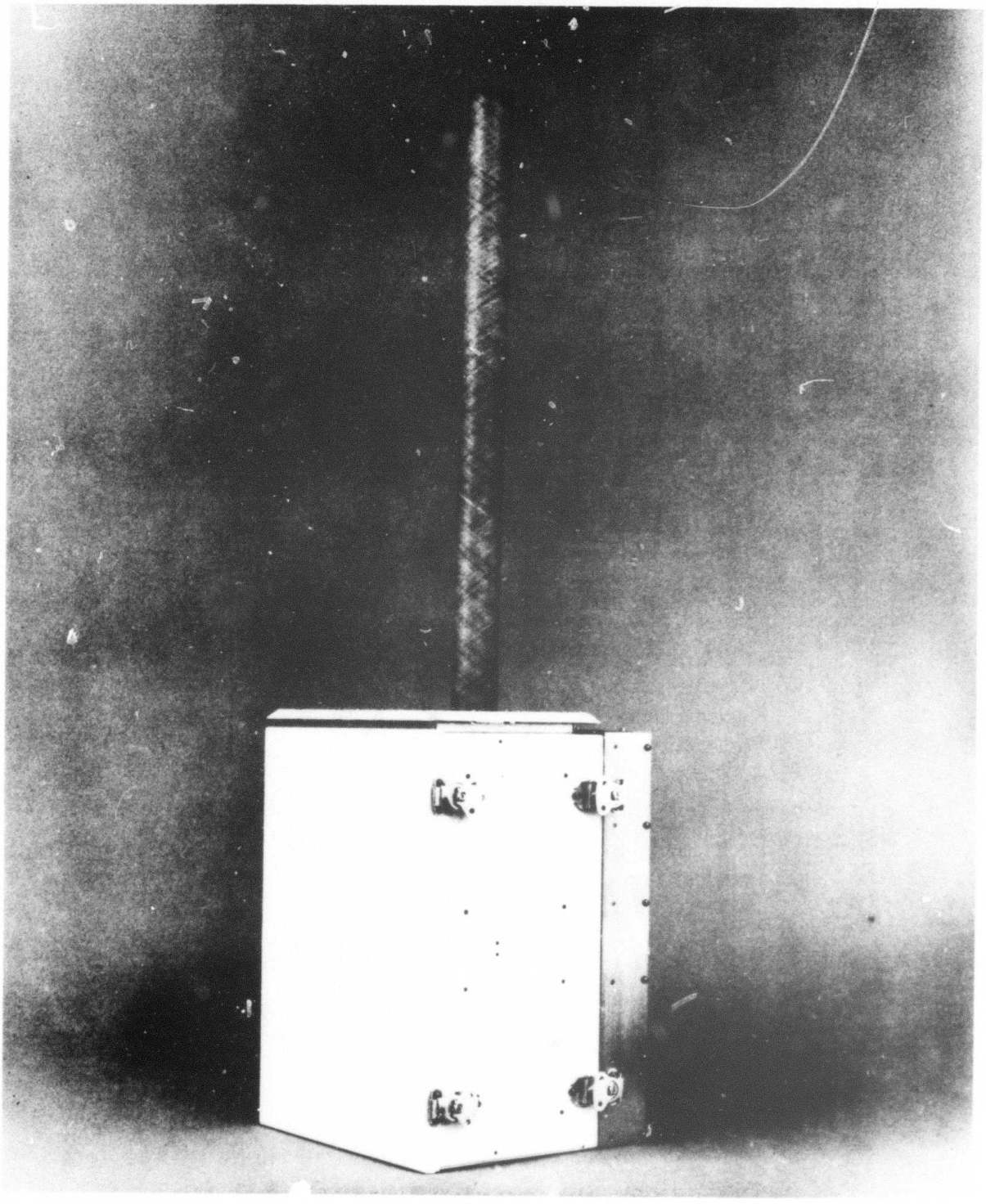

Figure 4-1. Experimental Repeater, Right Front View.

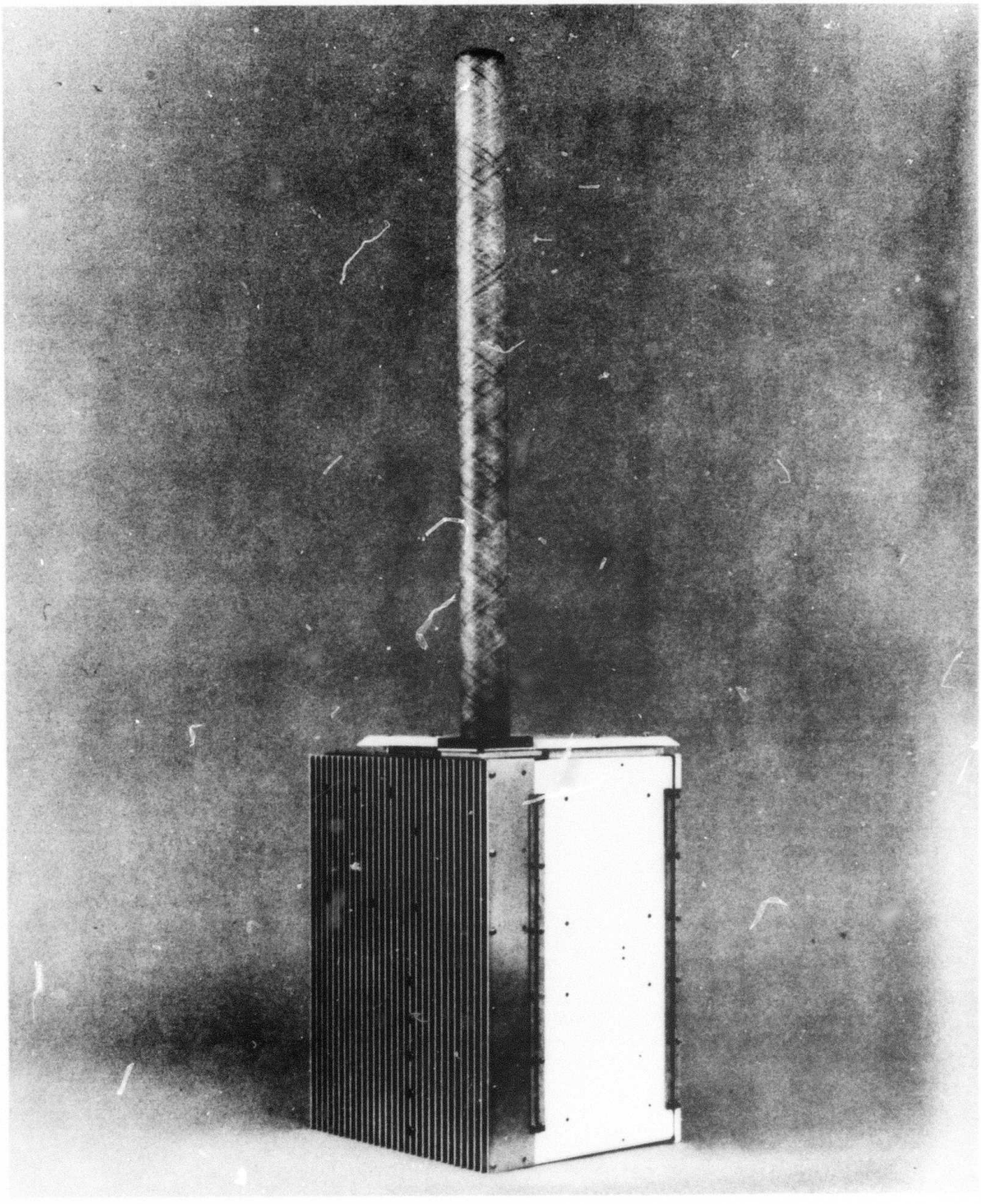

Figure 4-2. Experimental Repeater, Left Rear View.

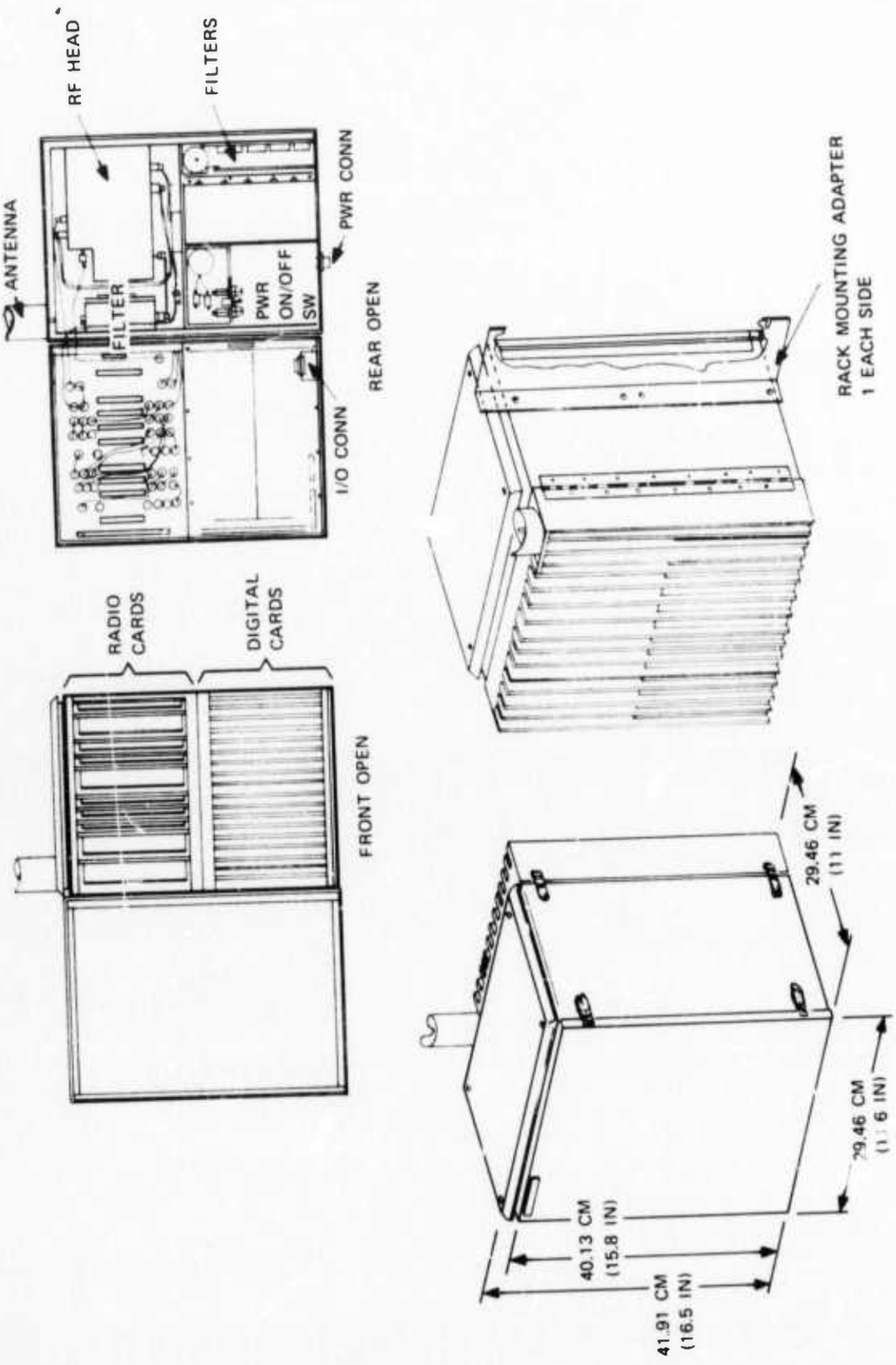

Figure 4-3. Detailed Drawing of Experimental Repeater.

5.1 INTRODUCTION

As we move into the final stages of development of the first experimental hardware and software for packet radio, it seems appropriate to take inventory of what hardware and software elements will be available and to clarify their functional capabilities. The term "Experimental Repeater" has been used to describe this equipment; however, this is a misnomer and is, in fact, too restrictive. Secondly, Fralick, in his latest note entitled "PRN Topics for Discussion," suggests that, in addition to our original terminology of terminal, repeater, and station, we adopt the term Packet Radio Unit (PRU), which is common to all network elements; and that we review and verify agreements on the original network element definitions.

Therefore, the purpose of this section is twofold. First, it is to briefly describe the functional hardware and software components currently being developed under the reference of experimental repeater, and to submit for consideration a functional description of this new PRU in terms of these hardware/software components. Second, it is to review the functional definitions of the original network elements, and to suggest some other elements that might be a part of a Packet Radio Network.

5.2 HARDWARE/SOFTWARE INVENTORY

The experimental hardware/software presently being developed has been called "an experimental repeater"; however, it might best be described as a group of hardware/software subelements or components. Figure 5-1 illustrates how this equipment might be partitioned, and is referred to as the initial equipment/software group. A brief functional description of each of these components follows.

a. Radio Transceiver. The radio transceiver consists of the transmitter and receiver which has a data detector at two different data rates. Its sole function is the conversion of digital packets into radio signals and vice versa. It is under the control of certain components in the digital section. Its connection to the other components is through the radio/digital interface and can be remoted up to 304.8 meters (1000 feet). The rest of the components, with the exception of the power distribution, have been lumped together and termed the "digital section." Dissecting this digital section reveals the CPU/memory control, direct memory access (DMA) channel, memory, radio I/O interface, I/O device channel, and software.

b. CPU/Memory Control. This includes the CPU microprocessor chips and the address decode hardware logic. It is the central processor to all other digital elements.

c. DMA Channel. Its function is the transfer of 16-bit parallel words between memory and its I/O ports. The radio transceiver uses three ports, one for transmit and two for receive. The DMA channel accesses memory on a cycle-stealing basis with the CPU given priority on memory cycles.

d. Memory. Its function is obvious and is partitioned into 1K words of PROM and 3K words of RAM.

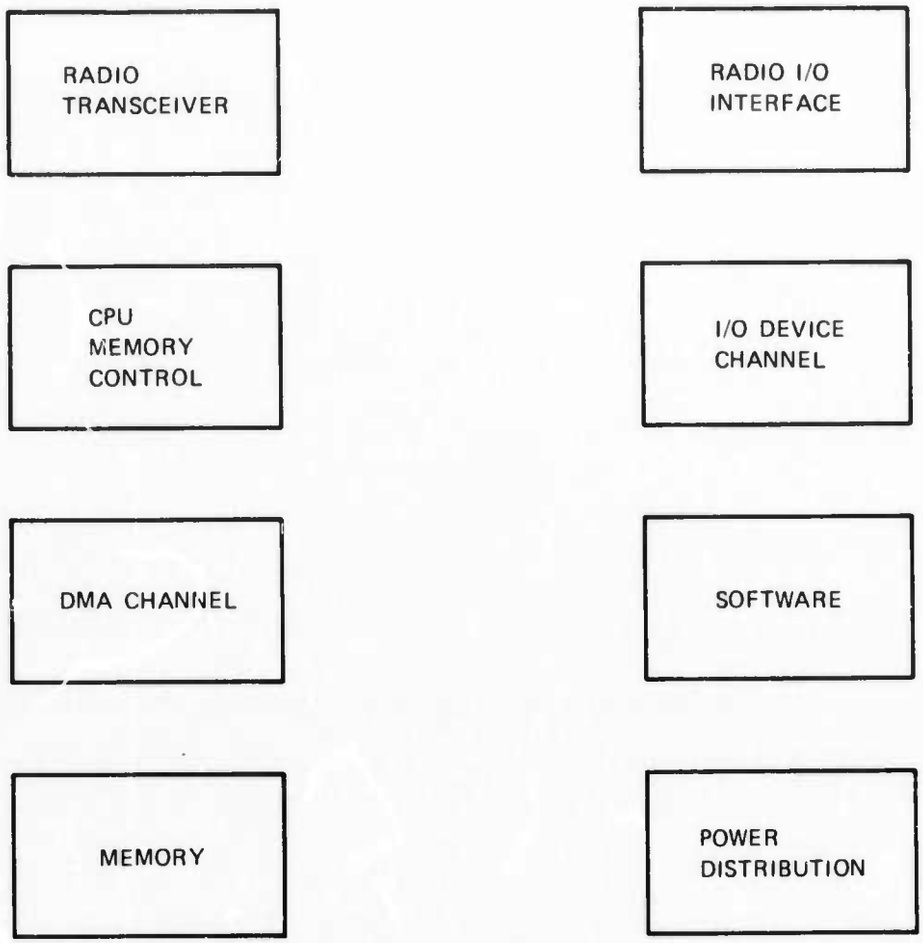

Figure 5-1. Initial Equipment/Software Group.

e. Radio I/O Interfaee. This is the hardware between the radio transeeiver and the DMA channel. It consists of two reeeive radio interfaees and one transmit radio interfaee. Its function is the eonversion between bit serial and 16-bit parallel and error eneoding/ decoding via a 32-bit eyclic redundant eoder/deeoder.

f. I/O Device Channel. This ehannel provides I/O to an I/O device via a serial EIA RS-232C or a current loop interfaee will aeeept baud rates of 110, 150, 300, and 1200. Its purpose is for software loading, diagnostie, and debugging aetivities.

g. Software. The software consists of an executive system and two independent programs called foreground and background processing. The transfer from one program to another is controlled by the executive system which also handles initialization and is interrupt-driven. Figure 5-2 illustrates this software structure. Foreground is where the actual packet processing and radio control takes palce. The background mode has the function of providing the device I/O and diagnostic capability to the processor.

Continuing the dissection process on the foreground mode produces two levles of packet handling. The first is called "high level software" and performs the logical decisions on routing and flow control, and directs the other level of packet handling which is called "low level software." This software is the actual doer in packet handling and is the controller of the radio, while the high level is the manager of packet handling. This distinction is important since it shows that the low level packet handling in the foreground processing is invariant to high level packet routing protocol and is common to all network elements.

h. Power Distribution. The power distribution converts +24 volts dc to all the required voltages needed for all the hardware components; however, it does not provide power for the I/O device channel or any I/O devices.

5.3 PRU DEFINITION.

Based on the initial equipment/software group components, the following are submitted as the components that make up the Packet Radio Unit (PRU). These include the following:

a. Radio transceiver
b. CPU/memory control
c. DMA channel
d. Radio I/O interface
e. Memory
f. Power distribution
g. Software
   1. Executive program
   2. Low level packet handling foreground program

The PRU is illustrated in figure 5-3.

The radio transceiver can be remoted from the other components with redundant power distribution for both the radio transceiver and digital equipment.

5.4 NETWORK ELEMENTS

The following is a discussion of the original network elements and others that have not been well defined.

a. Repeater. The sole function of a repeater is the extension of range between other network elements. For this reason, its function consists of the reception and retransmission of packets. It additionally applies error control and invokes packet routing protocol as dictated by the station. The repeater has no operational I/O requirements

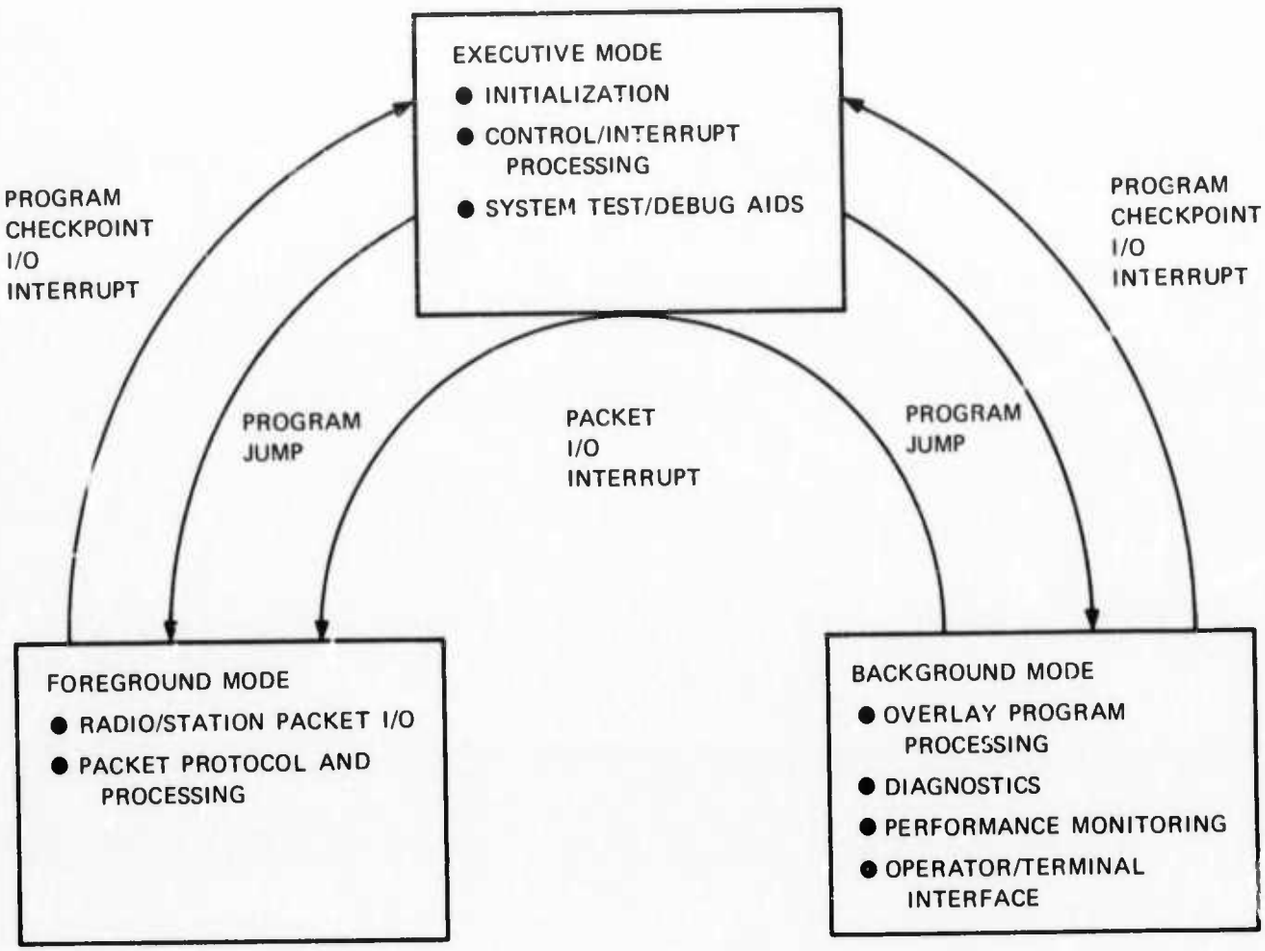

Figure 5-2. Software Structure.

from its processor. The basic components of the repeater are, in terms of our newly defined PRU, one PRU and the high level repeater initialization and routing protocol software as shown in figure 5-4. There would be no need to separate the radio transceiver from the other components and, therefore, all hardware is colocated.

b. Terminal (One I/O Device). A terminal is the user interface to the network and, therefore, its primary function is to make the network operation appear as transparent to the user as possible. This requires that the terminal have a PRU and an I/O device channel. In addition, it must have additional terminal software. This terminal software must perform the following tasks:

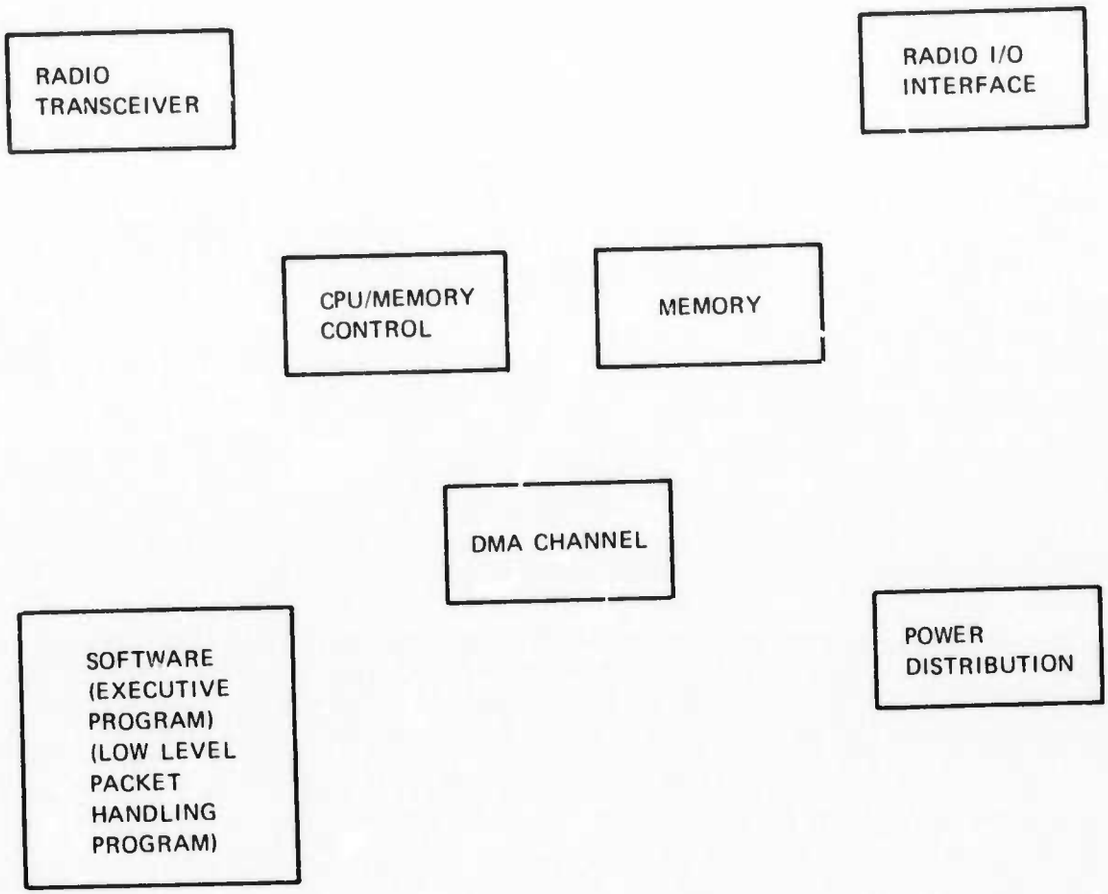

Figure 5-3. PRU Functional Components.

1. Initiate terminal to network
2. Take messages and build packets
3. Take packets and build messages
4. Initiate acknowledgments and other control packets
5. Interface and encode/decode messages to at least one I/O device including character positioning, cursor control, etc, up to 304.8 meters (1000 feet).

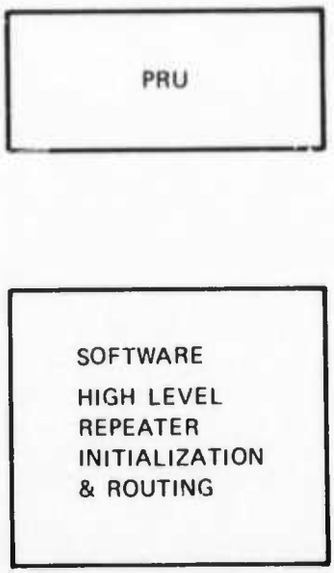

Figure 5-4. Repeater.

Figure 5-5 shows the functional components of a terminal, which are a PRU, I/O device channel, I/O device, power distribution for I/O channel, and terminal software.

The provision for remoting the radio transceiver from the rest of the PRU and remoting the I/O device from the I/O device channel should be available.

c. Station. The station is a multifunction network element. It has the responsibility for the network initialization, packet routing, and directory. It also is the gateway to the network, and must coordinate exogenous messages into the network and indogeneous messages out of the network.

The functional components that make up a station are:

1. PRU
2. Minicomputer
3. Two DMA channel ports
4. DMA channel interface to minicomputer
5. Station minicomputer software

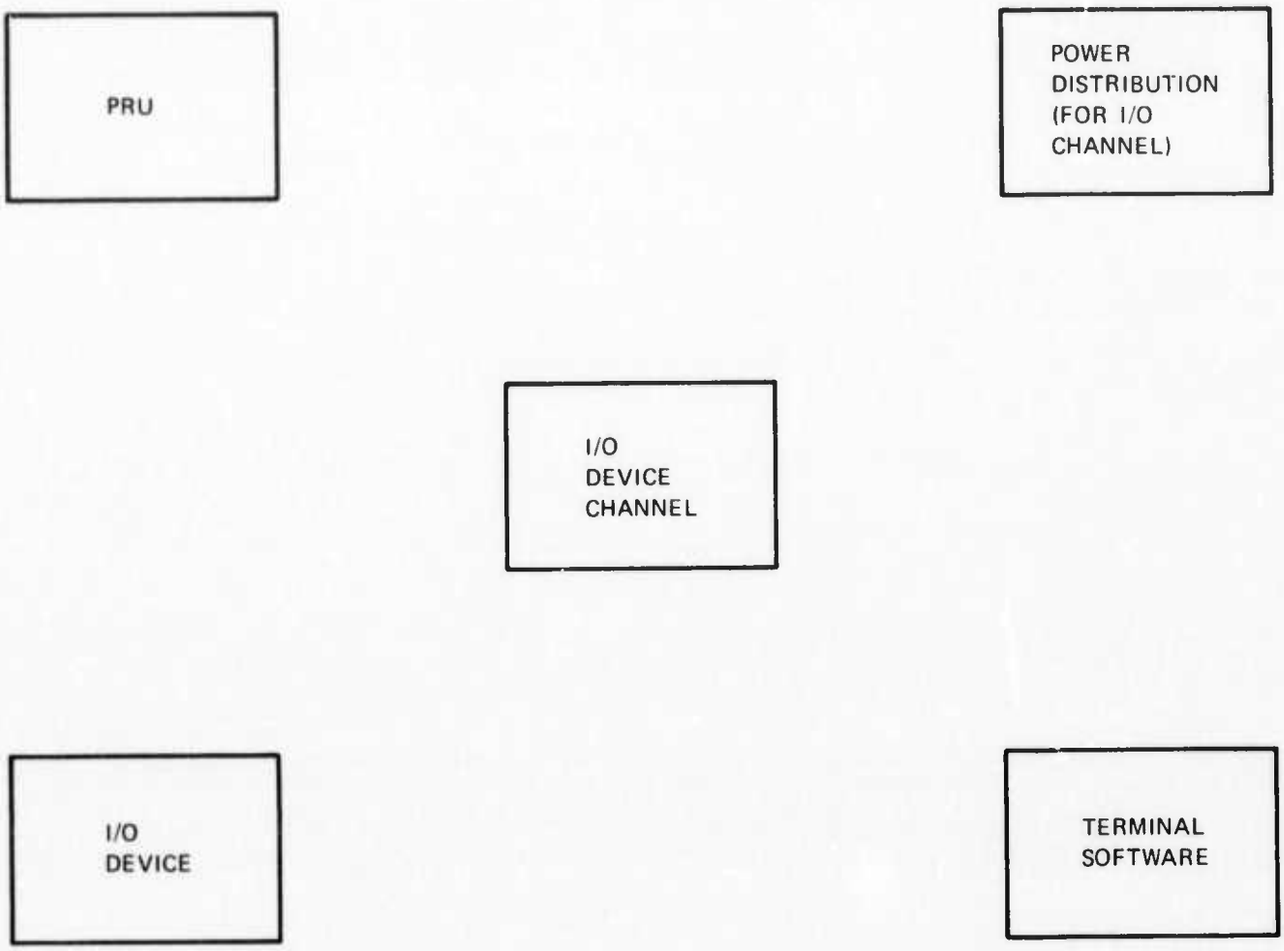

Figure 5-5. Terminal (One I/O Device) Functional Components.

6. High level microproeessor station software

7. Power distribution ot DMA ehannel interface.

The radio transceiver would be remoted from the rest of the PRU and the microprocessor and minicomputer would be within 15.24 metres (50 feet) of each other. The interfaee between the minieomputer and the PRU DMA channel ports would vary depending on the minicomputer. Figure 5-6 shows these functional components.

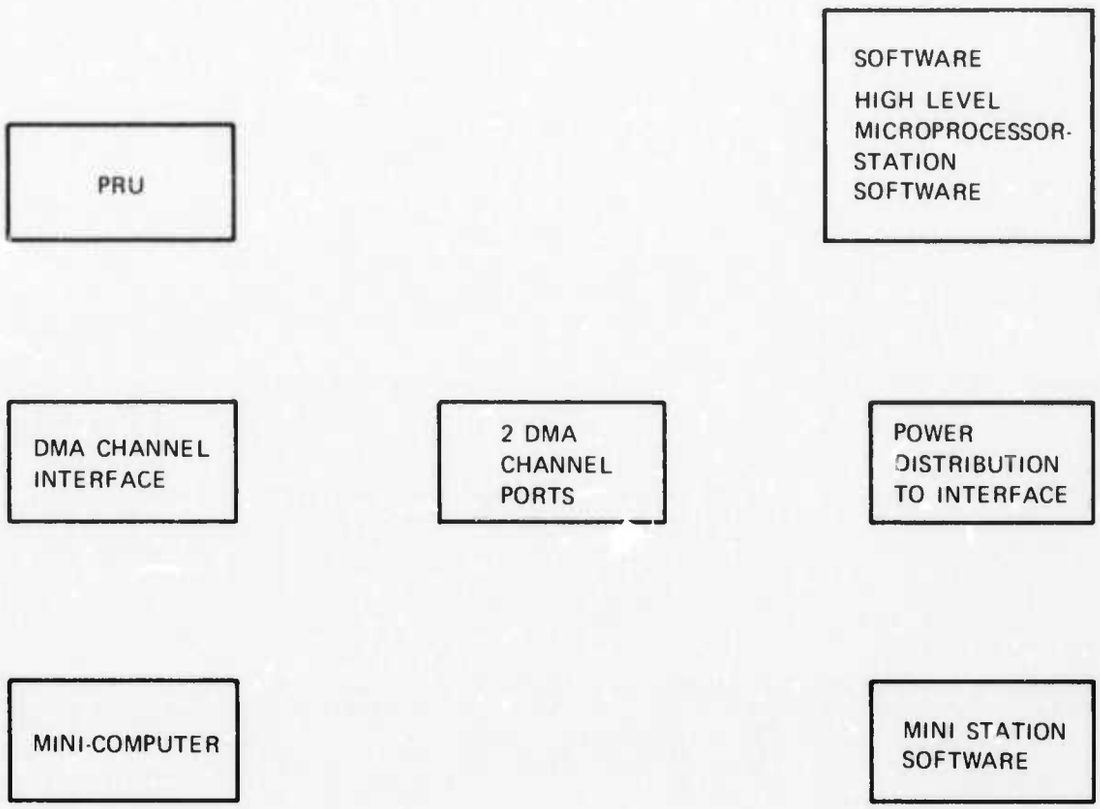

Figure 5-6. Station Funetional Components.

d. Drop Repeater (Repeater/Terminal). The drop repeater has the dual function of being both a repeater and a terminal. Its functional components are, therefore, the union of components of the terminal and repeater. These functional components are:

1. PRU
2. I/O device ehannel
3. I/O device

4. Software

   (a) High level repeater software

   (b) Modified terminal software

5. Power distribution to I/O channel

The terminal software would have to be modified since the initialization of a terminal to a repeater would be to itself. Figure 5-7 shows this configuration. The I/O device would be remote from the PRU (I/O device channel).

e. Multiple Terminal (I/O Devices). The terminal function has been described and the multiple terminal has the function of providing access to the packet radio network to more than one terminal. If multiple implies more than one and less than three, this could be handled by adding additional I/O device channels. Beyond three terminals, another configuration would be necessary.

This multiterminal configuration would contain a concentrator. The concentrator would have message buffers, and would decode serial data (RS-232C type) or output serial data to the terminal devices from the message buffers. The message buffers would be loaded from or dumped to the PRU via a DMA channel port. Thus, the PRU processor is relieved of servicing characters to/from multiple terminals and only service entire messages. The terminal devices could be remoted from the concentrator. The number of terminal devices that could be serviced would depend upon the data rates of the individual devices. The functional components are:

1. PRU

2. DMA channel interface

3. Concentrator

4. Software

   (a) High level packet handling software for PRU

   (b) Concentrator software

5. Power distribution for DMA I/O channel and concentrator

6. I/O terminal devices.

The components are shown in figure 5-8.

f. Multiple PRU Station. It has been suggested that one way to relieve the bottleneck congestion at the station would be to have multiple radio channel links that are spatially isolated via directive antennas. Each PRU would have its radio transceiver equipped with a directional antenna remoted from the other functional components of the PRU.

The interface to the station minicomputer would be identical to the single PRU station interface. The station minicomputer would have the additional task of coordinating packets to and from the various PRU's. The functional components are:

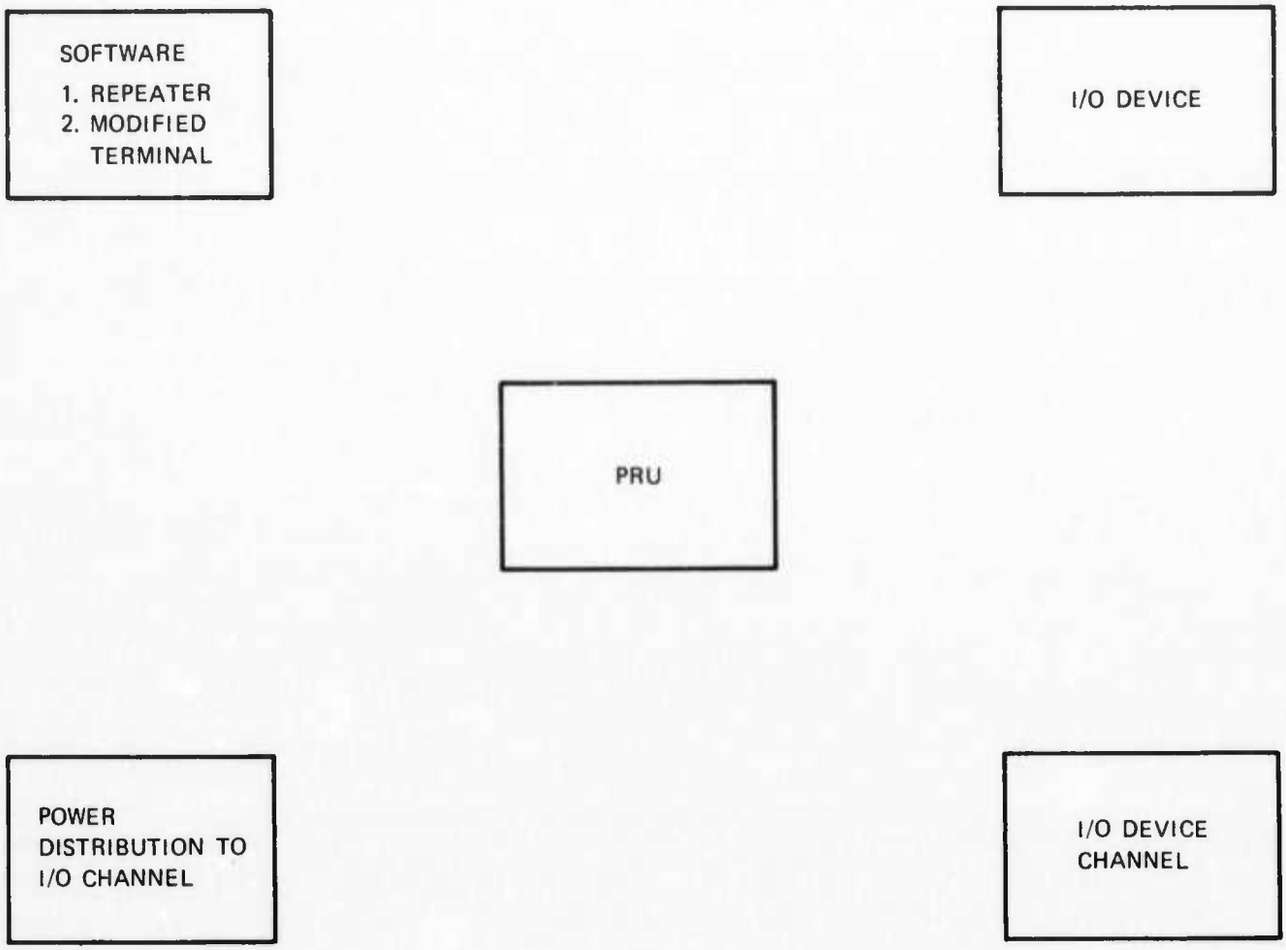

Figure 5-7. Drop Repeater Functional Components.

1. N number of PRU's with directive antennas
2. Minicomputer
3. 2N number of PRU DMA channel ports
4. N number of minicomputer to DMA channel interfaces
5. Software

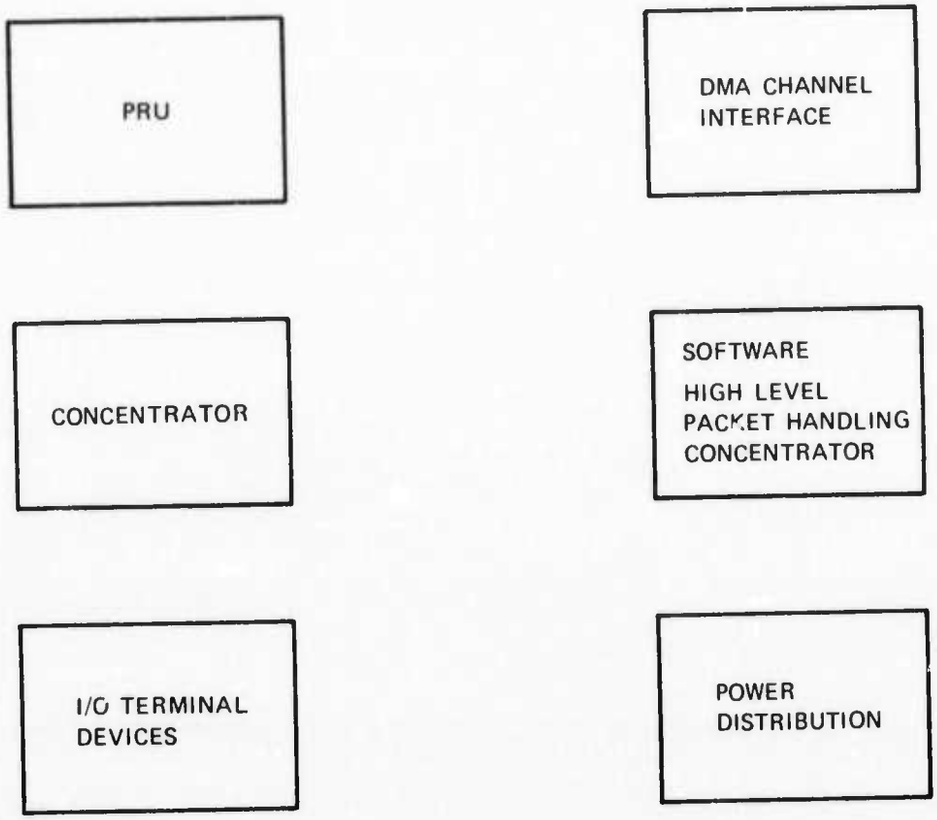

Figure 5-8. Multiple Terminal Functional Components.

(a) Minicomputer station software

(b) High level packet handling software for PRU's

6. Power distribution to DMA channel interfaces.

Figure 5-9 shows the interconnection of functional components.

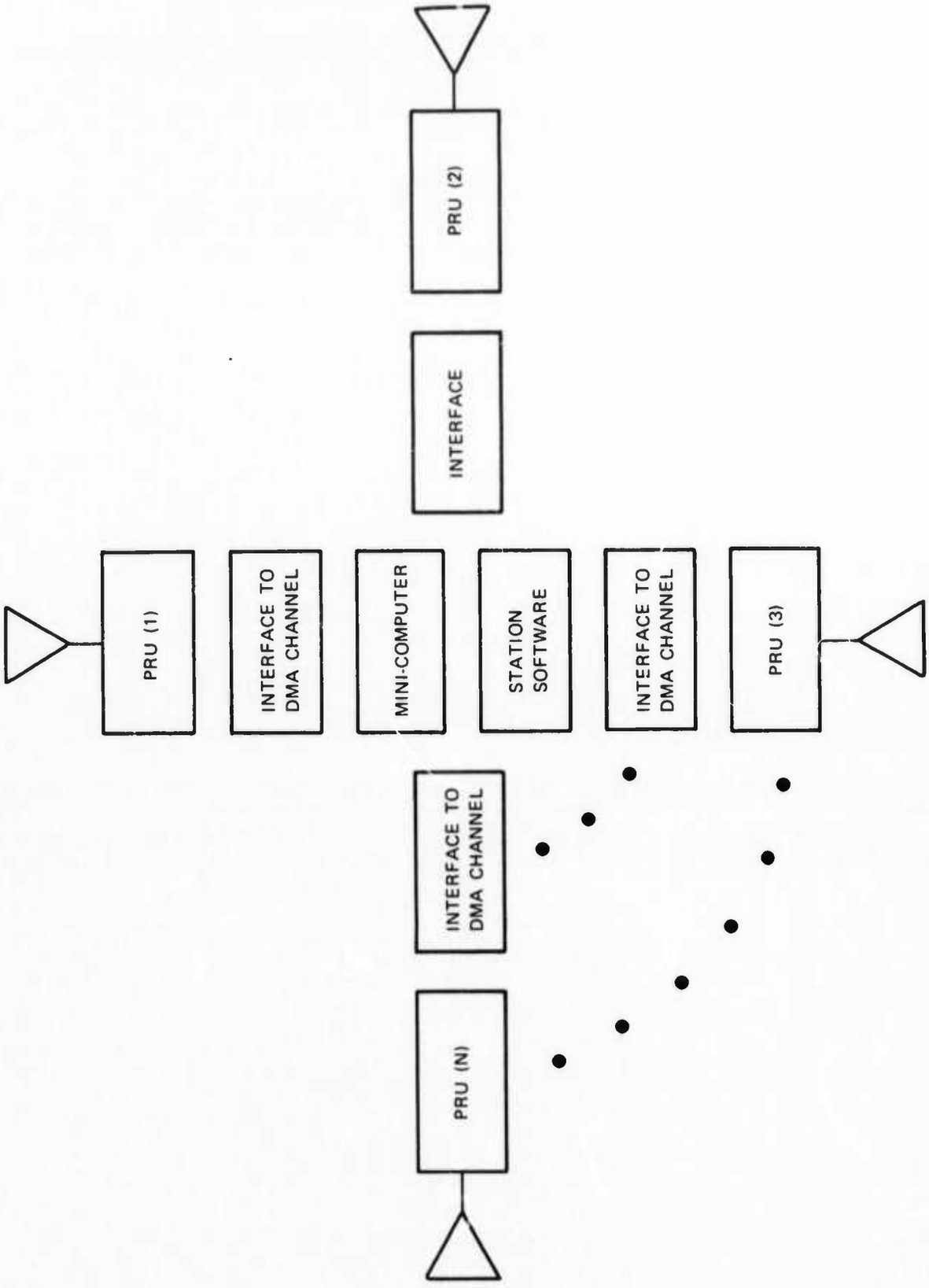

Figure 5-9. Multi-PRU Station.